ABSTRACT

In one embodiment, a state machine receives a plurality of instructions from an instruction register to be processed by a digital signal processor. After receiving a single RTI, the state machine loads each of the plurality of instructions one at time and determines the validity of each instruction. If the instruction is valid, the state machine transfers the instruction to the decoder. If the instruction is invalid or if a no-operation instruction is present, the state machine discards the instruction and immediately loads the next instruction.